Electronic Version
Stylesheet Version v1.1.1

[PROGRAMMABLE FREQUENCY DIVIDER WITH SYMMETRICAL OUTPUT]

Abstract

A programmable frequency divider circuit with symmetrical output is disclosed. The frequency divider includes a non-symmetrical LFSR based component operated in series with a symmetrical divider component. Both the LFSR and the symmetrical divider may be programmed to provide flexibility. The frequency divider can dynamically adjust the divisor of the LFSR component to overcome limitations in the divide resolution due to the series combination of dividers, providing even and odd divisor values. The divider architecture can also provide higher level functions, including synchronization of multiple divider outputs, dynamic switching of divisor values and generation of multi-phased and spaced outputs. The linear feedback shift register (LFSR) component includes a feedback logic network decomposed into multiple stages to realize a maximum latch-to-latch operational latency of one gate delay regardless of the size of the LFSR.